ABSTRACT OF THE DISCLOSURE

Provided are a control signal generation circuit and a method for generating a control signal controlled in units of bit time of a clock signal. The control signal generation circuit includes an input terminal, a first output terminal, and a second output terminal. The control signal generation circuit receives an input signal inputted to the input terminal in response to a clock signal and outputs a column latch signal and a data input/output command signal, which are separately activated and have a first time interval therebetween, to the first input terminal and the second input terminal, respectively, each in response to a test enable signal at a first state, or outputs the column latch signal and the data input/output command signal, which are separately activated and have a second time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal at a second state. The first time interval and the second time interval are controlled in units of bit time of the clock signal, and the second time interval is controlled to be smaller than the first time interval. The first time interval and the second time interval each amount to a time from when the column latch signal is activated to when the data input/output command signal is activated.

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